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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/990,093	11/21/2001	Jeffrey Binder	1303.65625	1287

7590 10/31/2006

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EXAMINER	
CHOWDHURY, SUMAIYA A	

ART UNIT	PAPER NUMBER
2623	

DATE MAILED: 10/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/990,093	BINDER ET AL.	
	Examiner	Art Unit	
	Sumaiya A. Chowdhury	2623	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 23-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18 and 23-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 8/11/06 have been fully considered but they are not persuasive.

(a) Applicant argues in regard to the Yokote reference, "does not describe a bus connection scheme that is capable of addressing the inventive memory array", on page 8, 2nd paragraph, of the Remarks filed 8/11/06.

Applicant did not explicitly claim a bus connection scheme; Applicant rather claimed the connection comprising at least two stream server processors, interconnect, arbitrator, etc.

(b) Applicant argues "The Examiner combines Rege to add the arbitrator, but the arbitrator of Rege does not show utility for a RAM system, and introduces latency by using a LAN to control and set up the arbitrator. This prevents the arbitrator of Rege from satisfying the 'near simultaneous access' to a 'large scale memory device' which are feature of Claim 1", on page 8, 3rd paragraph.

First, applicant does not claim that the arbitrator must have utility for a RAM system in claim 1. Secondly, the term "near simultaneous access" is a relative term having different meaning or degree to the skilled artisan.

(c) Applicant argues "Yokote is not capable of accessing 65 Gbytes of memory", on page 8, 4th paragraph.

Yokote teaches storing up to 6 GB of video data (col. 4, lines 1-11). The Examiner has brought in Haddad (2005/0097619) to teach this limitation.

(d) Applicant argues in regard to claim 18, "the Examiner cites the 'memory array address and logic 38' in Yokote as being the same as 'CPU running software.' To the contrary, a packet with a 'pause' command must be decoded, and acted upon, which is not the simple work of the Yokote 'addressing logic'", on page 8, 5th paragraph.

The Applicant only claimed means for responding to VCR type controls, said controls being handled by a separate CPU running software. Yokote teaches the memory array addressing logic 38 responds to controls such as pause, stop, rewind, and forward (VCR type controls). When a command such as a pause command is received, the logic 38 does not increment the current address for that user, but instead keeps generating the same address and hence the same block of data. Similarly, when a fast forward command is received, blocks of data are skipped in the forward direction.

(e) Applicant argues in regard to claim 5, "The Examiner appears to have confused capacity with throughput. Thompson does not describe anything about a specific size address bus, or a capacity greater than two Gbytes", on page 9, 3rd paragraph.

Applicant only claimed a large scale memory device having an address bus greater than 36 bits. Thompson teaches a system bus having adequate throughput

(e.g. 267 Mbytes to 1.2 Gbyte bandwidth). According to *The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition,* throughput is defined as "the total capability of equipment to process or transmit data during a specified time period; capacity".

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 6-8, 10-18, and 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yokote in view of Rege.

Regarding Claim 1, Yokote discloses a method for generating multiple parallel streams of data from a large solid-state mass storage device (Abstract). Yokote teaches, "a large scale memory device" by disclosing memory array 40 (Col. 3, line 48 - Col. 4, line 30). Yokote teaches, "means for storing said data in said large scale memory device" by disclosing memory array 40 receives input data through input ports 56 where the input data is provided from magnetic tape 18 or disk 20 (Col. 4, lines 12-30). Yokote teaches, "means for retrieving at least a portion of said data from said large scale memory device and generating multiple asynchronous streams of data" by disclosing output board 58 retrieves the video data from expansion board 50 and output board 58 transmits the video data through network 10 to terminal 12 (Col. 3, line 60 - Col. 4, line 35). Yokote teaches retrieving means includes, "means for generating

protocols necessary for the transport of each unique stream across at least one network and for decoding said unique streams of data" by disclosing logic modules 42, packet memories 44, and ATM/SONET interface modules 46, which perform the function of formatting the data into packets in accordance to a widely used standard (Col. 3, line 48, - Col. 5, line 25). Yokote discloses server 14 or "stream server processor", and VME bus 30 or "interconnect".

However, Yokote fails to explicitly disclose retrieving means including at least two stream server processors operatively connected to said large scale memory device and an interconnect allowing near simultaneous access to said data stored in said large scale memory device by said at least two stream server processors; including a hardware based arbitrator operatively connected to at least two stream server processors for controlling access to said large scale memory device so that multiple unique streams of data may be generated by one or more of said at least two stream server processors from said large scale memory device.

In a related art pertaining to video distribution, Rege teaches, "at least two stream server processors operatively connected to said large scale memory device" by disclosing servers 300 or "stream server processors" (Col. 3, lines 18-63). Rege teaches, "an interconnect allowing near simultaneous access to said data stored in said large scale memory device by said at least two stream server processors" by disclosing switch 400 or "interconnect" (Col. 3, line 18 - Col. 4, line 30). Rege teaches the switch or "interconnect" includes, "a hardware based arbitrator operatively connected to said at least two stream server processors for controlling access to said large scale memory

device so that said multiple unique streams of data may be generated by one or more of said at least two stream server processors from said large scale memory device" by disclosing arbiter 600 or "arbitrator" which is used to set the appropriate switching elements to allow content to be transferred from disks 800 to servers 300 via switch 400 (Col. 3, line 18 - Col. 4, line 67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yokote with the teachings of Rege in order to facilitate retrieving means including at least two stream servers, an interconnect that includes an arbitrator for the benefit of providing a multimedia delivery system which can dynamically balance the load over all the resources of the system .(Background - Rege).

As for Claim 2, Yokote teaches, "wherein the data stored and retrieved from said large scale memory device includes audio with a predetermined relationship to said video" by disclosing a solid state mass storage device capable of providing a large number of parallel data output streams on demand for multiple users (Col. 3, lines 12-27). Yokote further teaches video stored on memory array 40 is retrieved from tape 18 or disk 20 (Col. 4, lines 12-35). Yokote further discloses ATM stream generator can generate as many as 2,000 user-controllable data streams simultaneously (Col. 6, lines 1-12). Yokote discloses memory array is typically used for an on-demand video system, which typically includes video streams that comprise corresponding audio (Col. 3, lines 12-27).

As for Claim 3, Yokote teaches, "wherein said large scale memory device is comprised of random access memory" by disclosing data can be read and written to memory array 40 (Col. 4, lines 12-35). Therefore, memory array 40 reads on a large-scale memory device that is comprised of random access memory.

As for Claim 6, Yokote teaches, "wherein said audio and/or video data includes multiple unique programs" by disclosing a solid state mass storage device capable of providing a large number of parallel data output streams on demand for multiple users (Col. 3, lines 12-27). Since Yokote discloses a memory array for a video-on-demand system, the memory array therefore must store multiple unique programs.

As for Claim 7, Yokote teaches, "wherein said multiple streams of asynchronous streams of data are simultaneously generated from said multiple unique programs" by disclosing ATM stream generator 16 can generate as many as 2,000 user-controllable data streams or "unique programs" simultaneously (Col. 6, lines 1-12).

As for Claim 8, Yokote teaches, "means for allowing said stream(s) to be generated upon a first block of an audio/video program being stored in said large scale memory, without having to wait for entire said program to be written to said large scale

memory" by disclosing the video packets are sent to users continuously ensuring a constant data rate (Col. 5, lines 3-25).

As for Claim 10, Yokote fails to explicitly disclose solid-state memory array 40 comprises dual inline memory modules. The examiner gives Official Notice that it is notoriously well known in the art of video distribution to use dual inline memory modules as a form of memory to store multimedia content. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yokote in order for a large-scale memory device to be comprised of dual inline memory modules for the benefit of allowing more memory to be added to the system one chip at a time.

As for Claim 11, Yokote fails to explicitly disclose solid-state memory array 40 comprises DRAM. The examiner gives Official Notice that it is notoriously well known in the art of video distribution to use DRAM as a form of memory to store multimedia content. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yokote in order for a large-scale memory device to be comprised of dual inline memory modules for the benefit of storing up to four times more data compared to RAM.

As for Claim 12, Yokote fails to explicitly disclose solid-state memory array 40 comprises magnetic RAM. The examiner gives Official Notice that it is notoriously well

known in the art of video distribution to use magnetic RAM as a form of memory to store multimedia content. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yokote in order for a large scale memory device to be comprised of magnetic RAM for the benefit of MRAM chips can hold their content even when the chip loses power.

As for Claim 13, Yokote fails to explicitly disclose solid-state memory array 40 comprises dual data rate DRAM. The examiner gives Official Notice that it is notoriously well known in the art of video distribution to use dual data rate DRAM as a form of memory to store multimedia content. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yokote in order for a large scale memory device to be comprised of dual data rate DRAM for the benefit of using DDRDRAM to effectively double the clock frequency which in turn increases the data transfer rate of multimedia content.

As for Claim 14, Yokote fails to explicitly disclose solid-state memory array 40 comprises static RAM. The examiner gives Official Notice that it is notoriously well known in the art of video distribution to use static RAM as a form of memory to store multimedia content. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yokote in order for a large scale memory device to be comprised of static RAM for the benefit of SRAM holds data as long as there is enough power and provides data at faster rates compared to DRAM

As for Claim 15, Yokote fails to explicitly disclose solid-state memory array 40 comprises synchronous DRAM. The examiner gives Official Notice that it is notoriously well known in the art of video distribution to use synchronous DRAM as a form of memory to store multimedia content. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yokote in order for a large scale memory device to be comprised of synchronous DRAM for the benefit of SDRAM operates at higher clock speed compared to DRAM and therefore can deliver data at faster rates.

As for Claim 16, Yokote teaches, "wherein the protocol associated with said streams of data is generated in hardware" by disclosing ATM/SONET modules 46 (Col. 3, line 48 - Col. 4, line 35).

As for Claim 17, Yokote fails to explicitly disclose stream server processors are interconnected and shared across a backplane. In a related art pertaining to video distribution, Rege discloses in figure 2, servers 300 are interconnected across LAN 210 or "backplane" (Col. 3, lines 18-63). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yokote with the teachings of Rege in order for stream server processors to be interconnected and shared across a backplane for the benefit of providing a multimedia delivery system which can dynamically balance the load over all the resources of the system

(Background - Rege).

As for Claim 18, Yokote teaches, "means for responding to VCR type controls, said controls being handled by a separate CPU running software" by disclosing memory array addressing logic 38 (Col. 4, line 47 - Col. 5, line 35).

Claim 23 contains the limitations of claims 1 and 8 and is analyzed as previously discussed with respect to those claims.

Claim 24 contains the limitations of claim 2 and is analyzed as previously discussed with respect to that claim.

Claim 25 contains the limitations of claims 3 and 4 and is analyzed as previously discussed with respect to those claims.

Claim 26 contains the limitations of claim 17 and is analyzed as previously discussed with respect to that claim.

Claim 27 contains the limitations of claim 18 and is analyzed as previously discussed with respect to that claim.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yokote as applied to claim3 above, and further in view of Haddad (US 2005/0097619).

As for Claim 4, Yokote fails to explicitly disclose memory array 40 having a storage capacity of at least 65 gigabytes.

In an analogous art, Haddad teaches the memory 215 holds over 1300 gigabytes of data – [0052].

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to modify Yokote's invention to include the above mentioned limitation, as taught by Haddad, for the advantage of meeting the required load of the video on demand system.

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yokote in view of Rege as applied to claim 3 above, and further in view of Thompson (U.S. 5,881,245).

As for Claim 5, the combination of Yokote and Rege fail to explicitly disclose wherein said large-scale memory device has an address bus greater than 36 bits.

In a related art pertaining to video distribution, Thompson discloses MPEG stream server 502 or "large scale memory device" includes a system bus having adequate throughput (e.g., 267 Mbytes to 1.2 Gbytes bandwidth) (Col. 9, line 51 - Col. 10, line 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combination of Yokote and Rege with the teachings of Thompson in order for a large scale memory device to have an address bus greater than 36 bits for the benefit of facilitating quick data transfers between a large scale memory device and stream servers.

6. Claim 9 is rejected under 35 U.S.C 103(a) as being unpatentable over Yokote in view of Rege as applied to claim 3 above, and further in view of Youden et al. "Youden" (U.S. 5,815,146).

As for Claim 9, the combination of Yokote and Rege fail to disclose including a module CPU for each of said at least two stream server processors, each of said module CPUs using a first bus that is separate from a second bus from which said data streams are retrieved.

In a related art pertaining to video distribution, Youden discloses in figure 2, real time controller 60 or "CPU" comprises a first bus that connects with a plurality of data sources 100 and a second bus is connected to switch 70 (Col. 5, line 27- Col. 6, line 55).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yokote and Rege with the teachings of Youden in order to include a module CPU for each of said at least two stream server processors, each of said module CPUs using a first bus that is separate from a second

bus from which said data streams are retrieved for the benefit of generating and controlling thousands of video output streams at a relatively low-cost (Background - Youden).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sumaiya A. Chowdhury whose telephone number is (571) 272-8567. The examiner can normally be reached on Mon-Fri, 9-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Grant can be reached on (571) 272-7292. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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